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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/815,567	03/31/2004	Nigel C. Paver	MP1534	9397

68933 7590 03/21/2007

MARVELL-FHFGD
c/o FINNEGAN, HENDERSON, FARABOW, GARNETT et. al.
901 NEW YORK AVENUE
WASHINGTON, DC 20001-4413

EXAMINER	
CRIBBS, MALCOLM D	
ART UNIT	**PAPER NUMBER**
2115	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/21/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/815,567	PAVER, NIGEL C.	
	Examiner	Art Unit	
	Malcolm D. Cribbs	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 December 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-23 are presented for examination.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Clabes et al [Publication No. US 2004/0159904] in view of Pate [Publication No. US 2004/0080717] in further view of Watts [Patent No. US 5,996,084].

As per claim 14, Clabes teaches the invention comprising:

analyzing operation of a chip executing an application including sensors to detect an existence of a power consumption property [temperature exceeding a specific threshold] set at a predetermined value [Page 1, paragraph 0005; it would be inherent that the chip is executing an application which causes the increase of the temperature on the chip].

Clabes discloses a method of detecting temperature of a chip above a threshold, thus eliminating high temperature situations. However, Clabes does not disclose a

method of recording a time that the sensors output indicates an existence of a power consumption property at a predetermined value.

Pate teaches a method of controlling the temperature of a high temperature component wherein if the temperature exceeds a certain threshold an appropriate action to reduce the temperature. Pate discloses monitoring sensor outputs of a sensor [Fig. 4, 5, and 6 thermal sensor mechanism] wherein each sensor output to indicates a measurement of the power consumption property [Page 4, [0036]], and records a time that each of the outputs [Fig. 5 and 6, thermal sensing mechanism's] indicates an existence of the power consumption property [the amount of time the temperature is greater than a threshold temp T_2 is recorded] at a corresponding measurement [Page 2, [0020]].

It would have been obvious to one of ordinary skill in the art to combine the teachings of Clabes and Pate because they both teach methods of compensating for high temperatures by taking appropriate action due to excess temperature readings using temperature sensors. One of ordinary skill in the art would be motivated to make this combination of including the ability to record the amount of time an excess temperature exist as taught by Pate, as doing so would give the added benefit of determining the end of the useful life of the high-temperature component and prevention of damaging the chip due to excessive temperatures for extended periods of time [Page 3, paragraph 0026].

Clabes and Pate do not teach monitoring the application and correlating the event data with parts of the application.

Watts discloses another method of compensating for high temperature by taking appropriate action due to excess temperature readings using temperature sensors. Watts teaches:

monitoring one or more parts of an application [Col 3 lines 1-10; Col 13, lines 7-9; wherein CPU activity is monitored which includes application software program currently active];

and for at least one of one of the parts of the application, correlating the event data with the at least one of the parts of the application [Col 13 line 54 – Col 14 line 12; wherein the instructions of the CPU are compared to a look-up table and further correlated with thermal conditions to determine if a thermal level will be reached while processing the instructions]; and

a performance analyzer on a second node, the performance analyzer communicatively coupled to the circuitry on the first node to use the correlated information [it is inherent to have an analyzer to use the correlated information to determine is a thermal level will be reached while processing the instructions].

It would have been obvious to one of ordinary skill in the art to combine the teachings of Clabes and Pate with Watts because they teach methods of compensating for high temperatures by taking appropriate action due to excess temperature readings

using temperature sensors. One of ordinary skill in the art would be motivated to make this combination of including the ability to correlate temperature data with parts of an application as taught by Watts, as doing so would give the added benefit of determining, based on applications of a CPU, whether a CPU should rest based upon the activity level, and also provides real-time reduction and restoration of clock speeds in response to managing applications of the CPU.

As per claims 2, 10, and 15, wherein the power consumption property of the chip comprises temperature, and the temperature comprises a temperature range including one or more temperatures [Pate; Fig. 2, temperature range T_1 to T_2].

As per claims 3, 11, and 16, wherein each sensor output corresponds to a temperature range, and indicates the existence of the one or more temperatures measured at the corresponding sensor output [Pate; Fig. 2, temperature range T_1 to T_2 wherein the temperature range is read using temperature sensors].

As per claims 4, 12 and 17, wherein the power consumption property of the chip comprises voltage drop, and wherein the voltage drop range includes one or more voltage drops [Watts; wherein Watts discloses based on the activity of the applications of the CPU, adjusting the performance of the CPU based on thermal conditions or power consumption which is directly proportionate to voltage].

As per claims 5, 13, and 18, wherein each sensor output corresponds to a voltage drop range, and each sensor output indicates the existence of a voltage drop measured at the corresponding output [Watts; wherein Watts discloses based on the activity of the applications of the CPU, adjusting the performance of the CPU based on thermal conditions or power consumption which is directly proportionate to voltage].

As per claim 1, Clabes discloses the invention comprising:

analyzing operation of a chip executing an application including sensors to detect an existence of a power consumption property [temperature exceeding a specific threshold] set at a predetermined value [Page 1, paragraph 0005; it would be inherent that the chip is executing an application which causes the increase of the temperature on the chip].

Clabes discloses a method of detecting temperature of a chip above a threshold, thus eliminating high temperature situations. However, Clabes does not disclose a method of recording a time that the sensors output indicates an existence of a power consumption property at a predetermined value.

Pate teaches a method of controlling the temperature of a high temperature component wherein if the temperature exceeds a certain threshold an appropriate action to reduce the temperature. Pate discloses monitoring sensor outputs of a sensor [Fig. 4, 5, and 6 thermal sensor mechanism] wherein each sensor output to

indicates a measurement of the power consumption property [Page 4, [0036]], and records a time that each of the outputs [Fig. 5 and 6, thermal sensing mechanism's] indicates an existence of the power consumption property [the amount of time the temperature is greater than a threshold temp T_2 is recorded] at a corresponding measurement [Page 2, [0020]].

It would have been obvious to one of ordinary skill in the art to combine the teachings of Clabes and Pate because they both teach methods of compensating for high temperatures by taking appropriate action due to excess temperature readings using temperature sensors. One of ordinary skill in the art would be motivated to make this combination of including the ability to record the amount of time an excess temperature exist as taught by Pate, as doing so would give the added benefit of determining the end of the useful life of the high-temperature component and prevention of damaging the chip due to excessive temperatures for extended periods of time [Page 3, paragraph 0026].

As per claims 6-8, it is directed to the method of steps to implement the system as set forth in claims 14-18. Therefore, it is rejected for the same basis as set forth hereinabove.

As per claims 9-13, it is directed to an apparatus to implement the system as set forth in claims 14-18. Therefore, it is rejected for the same basis as set forth hereinabove.

As per claims 19-23, it is directed to a machine-readable medium to implement the method of steps as set forth in claims 14-18. Therefore, it is rejected for the same basis as set forth hereinabove.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Malcolm D. Cribbs whose telephone number is 571-272-5689. The examiner can normally be reached on M-F 8AM-430PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas Lee can be reached on 571-272-3667. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Malcolm D Cribbs
Examiner
Art Unit 2115

March 19, 2007
MC